Date: 01/03/2020

EIC Detector R&D Progress Report

Project ID: eRD24__
Project Name: A Proposal for Silicon Detectors with high Position and Timing Resolution as Roman Pots at EIC
Period Reported: from 7/2029 to 12/2019
Project Leader: _____
Contact Person: E.C. Aschenauer (BNL), A.Tricoli (BNL)

Project members
E.C. Aschenauer (BNL), A.Tricoli (BNL), A. Jentsch (BNL), S. Fazio (BNL), A. Kiselev (BNL), G. Giacomini (BNL), C. Da Via (SBU/Manchester)

Abstract

Roman Pots are an integral part of the detector system of an EIC and essential for the success of its physics program. Roman Pots will provide a critical contribution to the study of exclusive production processes in ep collisions, i.e. deeply virtual Compton scattering as well as double tagging with deuteron in eA interactions, among others. This proposal aims at setting the performance requirements for a Roman Pot detector at EIC, focusing on spatial granularity, timing resolution and acceptance. In addition, an innovative silicon-based technology, called Low Gain Avalanche Diode (LGAD), will be studied as it has the potential to combine in a single sensor fine spatial resolution and precise timing. More specifically, the AC-coupled version of LGADs (AC-LGADs) will be studied and prototypes fabricated at BNL to establish spatial and timing performance as well as the minimal possible inactive area that is critical for placing such sensors as close as possible to the beam. The performance of AC-LGADs will be compared to alternative sensors too.

Past

What was planned for this period?

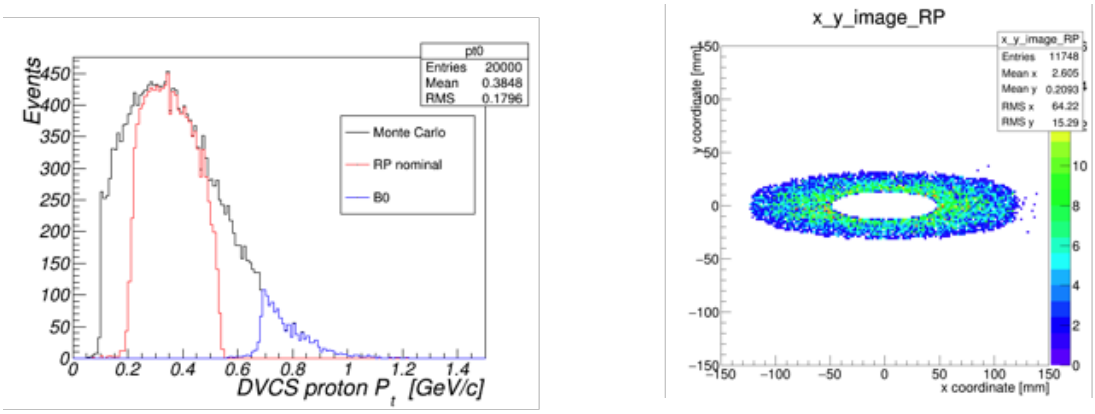
In this period it was planned to study the physics requirements for the Roman Pot detectors at an EIC. More specifically it was planned to establish a general layout of the detector in terms of sensing area, as well as the necessary spatial and timing resolution to achieve the required physics performance. Furthermore, we planned to design AC-LGAD wafers to be then fabricated at BNL in following period, such that the physics and performance requirements could be met.

What was achieved?

In this first period we defined a set of requirements for geometrical layout (including the non-active region of the Si-sensors) - such that the acceptance of the forward scattered particles is not impacted - and the timing resolution. For these studies, three proton beam energies were considered (275 GeV, 100 GeV, 41 GeV), along with the corresponding beam parameters (e.g. transverse beam size or "sigma", angular divergence, etc.). Physics simulations were carried out using the DVCS event generator MILOU combined with EicRoot comprising a full GEANT model of the IR. From these studies, baselines for the needed active sensitive area to achieve full acceptance, and conservative estimates for expected momentum smearing for proton reconstruction from exclusive processes were established. Figure 1 below shows the scattered proton transverse momentum acceptance for the 100 GeV case and illustrates the effect of adjusting the divergence of the beam on the low-pT portion of the spectrum. The central hole seen in the left column plots of Figure 1 is the 10 sigma (transverse beam size) safe distance required to protect the sensors from damage from the beam. The different beam configurations change this safe distance by altering the beta functions of the beam at the Roman Pot location. Figure 1 also illustrates the need for an active sensitive area of around 25 cm x 10 cm to achieve the full acceptance for all energies, with the higher (275 GeV) energy having a less demanding horizontal requirement (~20cm).

In order to obtain reasonable estimates for momentum resolution in the Roman Pots, several effects were considered including the pixel size of the sensor, the effect of the beam angular divergence, and the effect of the finite bunch length being rotated by the crab cavity. Table 1 shows the summarized values of smearing in momentum from the angular divergence and primary vertex uncertainty from the rotation of the bunches by the crab cavity, while Table 2 shows the effects on the smearing in momentum from various choices of silicon pixel size. These various sources add in quadrature to give the overall worst-case smearing of ~45 MeV/c for the 275 GeV beam, ~23 MeV/c for the 100 GeV beam, and 15 MeV/c for the 41 GeV beam. The smearing from the beam angular divergence is essentially fixed and given by the beam parameter itself, where we have used the angular divergence values for the high divergence configuration in order to place upper bounds on the smearing in momentum. The smearing from the finite bunch length is dependent on the actual length itself (currently ~ 10cm). This smearing in momentum from the crab cavity rotation of the bunches can be corrected with precise timing ~30ps. The ideal pixel size would be the smallest possible values we tested (250um x 250um), but as is seen in Table 2, one could live with larger pixels with little effect on the final smearing. Figure 2 illustrates the comparison of the reconstructed t-distribution to the one generated by MILOU. The dip seen in both plots is due to the acceptance gap between the B0 dipole sensors and the Roman Pot sensors as shown in Figure 1 (note: no acceptance correction has been applied). In the low-t (from Roman Pots) and high-t (from B0) portions of the distribution, the reconstruction from the full GEANT simulation matches well with the generated distribution.

High Divergence – High luminosity – Low Acceptance configuration



Low Divergence – Low luminosity – High Acceptance configuration

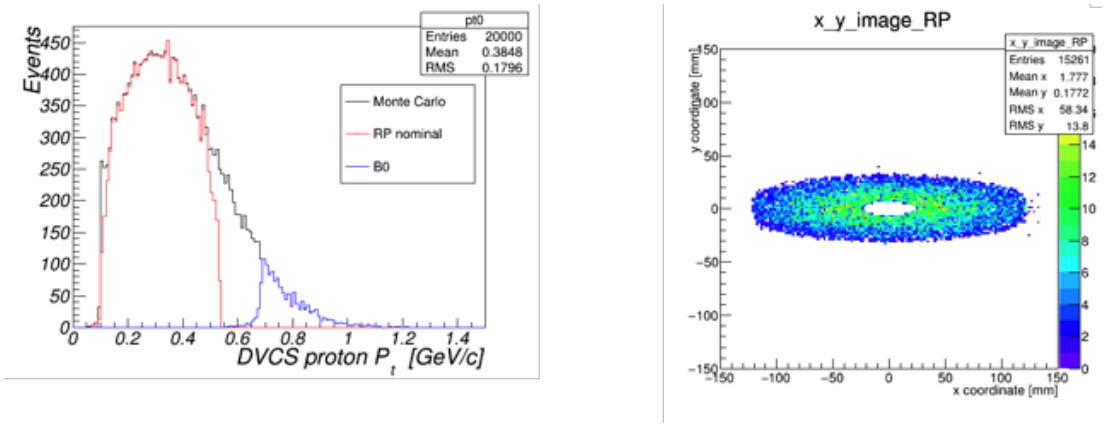


Figure 1: DVCS proton transverse momentum acceptance plots (left column) showing acceptance for Roman Pot sensors (red) and B0 dipole sensors (blue) compared to the generated MC tracks (black). The top row is a beam configuration that maximizes luminosity with reduced acceptance, and the bottom row maximizes acceptance with lower luminosity. The second column shows the acceptance "image" on the first Roman Pot sensor, displaying the needed active area to capture all of the scattered DVCS protons.

Beam Energy	δp_t from Angular Divergence [MeV/c]	δp_t from Crab Rotation [MeV/c]
275 GeV	40	20
100 GeV	22	9
41 GeV	14	10

Table 1: Smearing in transverse momentum from angular divergence and rotation of proton bunch in crab cavity.

Beam Energy	250um x 250um pixel [MeV/c]	500um x 500um	1mm x 1mm
275 GeV	18.5	20.6	26.9
100 GeV	8.5	9.2	11.9
41 GeV	8.0	10.0	11.5

Table 2: Smearing in transverse momentum from various possible silicon pixel sizes for the Roman Pot sensor.

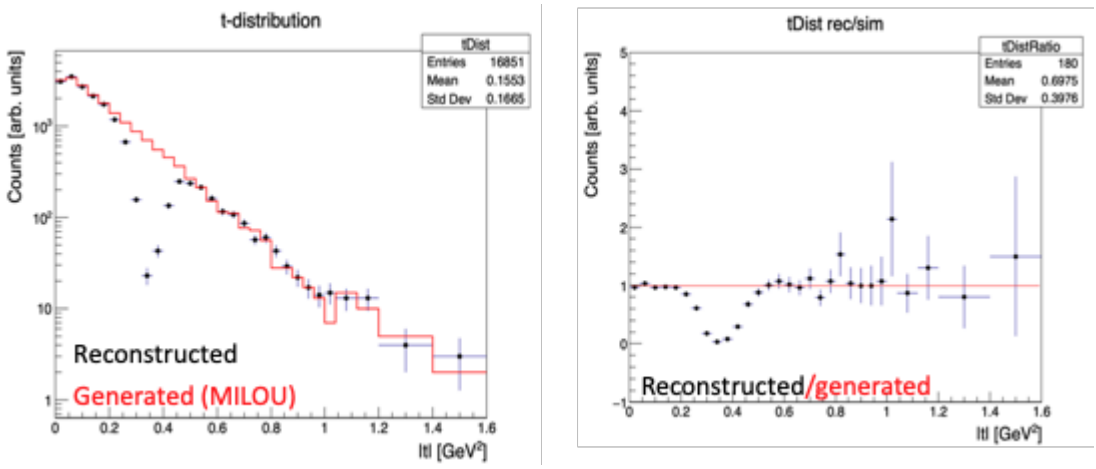


Figure 2: The left plot shows the reconstructed (black) and generated (red) |t|-distributions for the 100 GeV DVCS scattered protons. The right plot shows the ratio of the two, where the "dip" is coming from the acceptance gap between the Roman Pots sensors and the B0 dipole sensors.

In this period we also continued the characterization of AC-LGADs that were previously fabricated at BNL. More specifically, we studied time resolution of AC-LGADs compared to the one of standard, i.e. DC-coupled, LGADs, and we studied the AC-LGAD response to different particle beams such as beta particles, X-rays, gamma-rays, red and infrared laser beams as well as neutrons.

Using beta particles from ^{90}Sr source, X-rays from ^{241}Am source, gamma rays and neutrons from ^{252}Cf source, as well as high energy neutrons from a Deuterium-Tritium generator, we measured the time jitter (defined as the ratio between noise and slew rate (dV/dt)) in AC-LGADs with pixels of 200 x 200 um^2, and we found it to be approximately 20 ps that is compatible with the jitter measured in LGADs with 1 x 1 mm^2 pads for High Luminosity LHC (HL-LHC) experiments. The gains of the AC-LGADs tested are in the range of 15-25, as measured with X-rays.

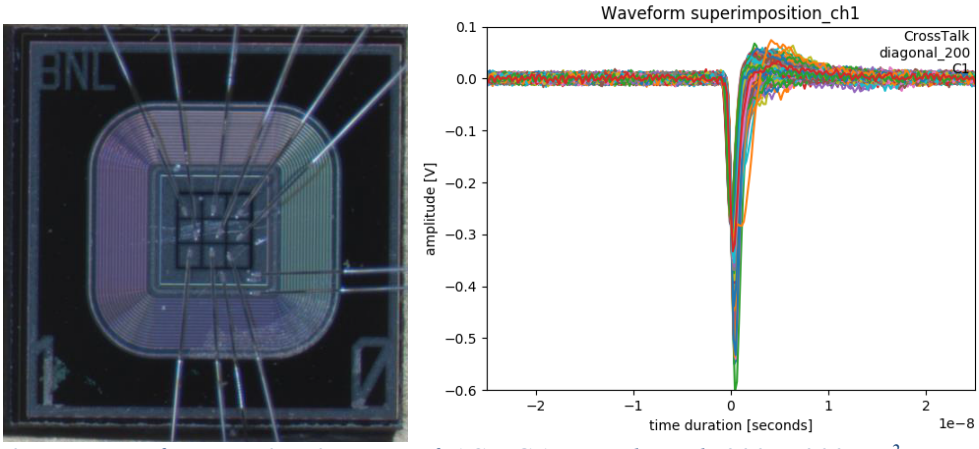


Figure 3: Picture of a BNL 3 x 3 array of AC-LGAD pixels with 200 x 200 um^2 area (left). Signal waveforms generated by beta particles from ^{90}Sr source on an AC-LGAD pixel (right) for the sensor pictured on the left.

Other studies focused on the charge sharing across neighbouring pixels of different sizes and geometries and the uniformity of the charge collection. Figure 4 below shows the charge collection on pixel and strip sensors using an infrared beam injected in the unmetalized area between pixels/strips, using the Transient Current Technique (TCT), in which a scan of the sensor area is performed by the laser beam with micron precision. Figure 4 also shows the charge sharing across pixels and strips. In the strip sensor it is measured that the neighbouring strips collect 13%, 6% and 4% of the charge of the illuminated pixel the farther away the strips are from it. The charge sharing properties of AC-LGADs can be used to further improve spatial resolution at a given pixel/strip pitch, and will be studied in greater detail in the next period with new wafers.

In Figure 4 also visible is a collateral effect of charge sharing across the edges of the sensors due to a resistive path on the electrode terminations. This effect has been studied with the previous sensor batch and will be corrected in the next wafer production.

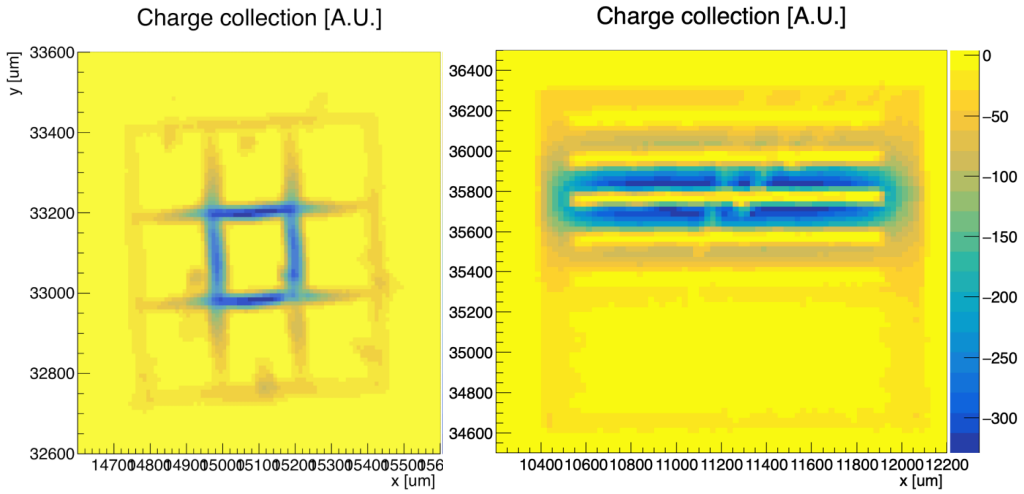


Figure 4: Charge collection (in arbitrary units) in AC-LGAD pixel (left) and strip (right) sensors using an infrared laser using the TCT scanning method. The pixel sensor is the one pictured in Figure 3, while the strip sensor is made by 8 strips with 200 um pitch, 1.5 mm long.

Based on the above-mentioned results, we performed TCAD studies of new and optimised designs of AC-LGAD sensors, specifically for application in Roman Pots at EIC. For example we studied in simulation the impact of the position and distance from the active area of guard rings to establish minimum edge size for safe operations at EIC.
For example, at BNL we use to place only one floating guard ring (GR) around pads fabricated on standard high-resistivity 300-um thick wafers. This GR, characterized by certain dimensions and metal field plate extension, has proven to sustain voltages in excess of a few hundred Volts. TCAD simulations show that such spacing is inadequate for thin wafers, and the floating GR must be placed much closer to the (grounded) active area. This is fortunate, since it helps in shrinking down the dead area external to the active region to about 50 to 100 um.

Besides TCAD simulations, on LGAD fabrication batches we put several test structures of the kind shown in Figure 5. They consist of a central pad, grounded during the I-V sweep (high voltage is applied on the back of the handling wafer, a low resistivity Czochralski (CZ) p-type wafer on which 50-um epitaxial high resistivity layer has been grown). Surrounding the central pad, there is a series of one or more GRs, to control the high voltage at the periphery of the device and prevent breakdowns. In Figure 3, a device with only one GR is shown. In a wafer, there have been placed several structures with only one GR, and they differ for the extension of the metal Field Plate, FP (5, 7 or 9 um) and for the distance between the n-implants of the central pad and the GR (10, 12 and 15 um). I-V curves are shown in Figure 6: it can be seen that all these structures with only one GR can sustain voltages higher than 400 V, except for the structures with a distance between implants of 10 um. It must be noted that LGADs fabricated at BNL have operation voltages as low as 160 V, which makes all the combinations FP extension/implant distance suitable as termination.

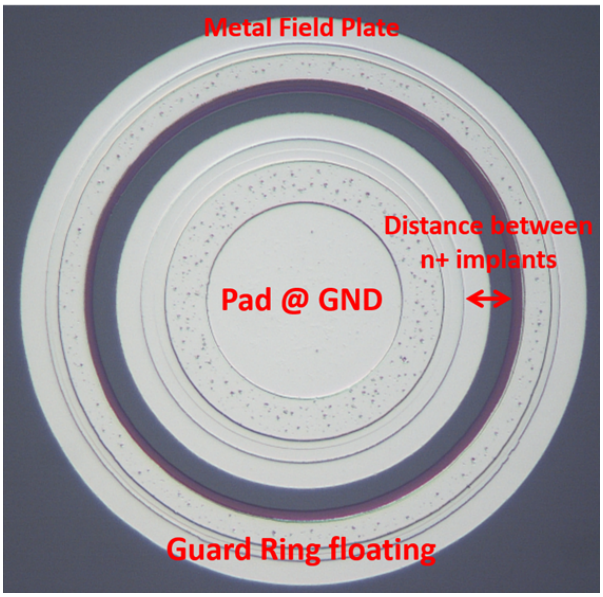


Figure 5: Example of test structure for high voltage handling capability tests. The central pad is grounded during measurement and it is surrounded by one guard ring only.

The distance between the n+ of the grounded pad and the floating GR-metal-end can therefore be about 35-40 um (mainly due to photolithographic constraints). Outside the GR, a termination must be placed, since a simple cut of the device by means of a diamond saw or a laser dicing would inject into the active area high spurious currents. A trench can be added, whose surface – after proper passivation – contributes minimally to the current. We performed some tests with trenches etched by a Reactive Ion Etching (RIE) technique: a profile of etched silicon is shown in Figure 7. Even in the case of an isotropic etch (wet-etch or RIE), the trench is expected to

extend laterally as much as the depth of the substrate, i.e. 50 um. A slim edge in the order of 100 um is therefore already within reach.

To test trench functionality as a slim edge (particularly, passivation techniques and resulting leakage currents), we started the fabrication of a few wafers by ion-implanting test structures (such as diodes) only. Trenches will be etched at several distances from pads and different passivation methods will be compared. Such passivation methods will be, for example, thermal oxidation, PECVD oxide deposition, etc.

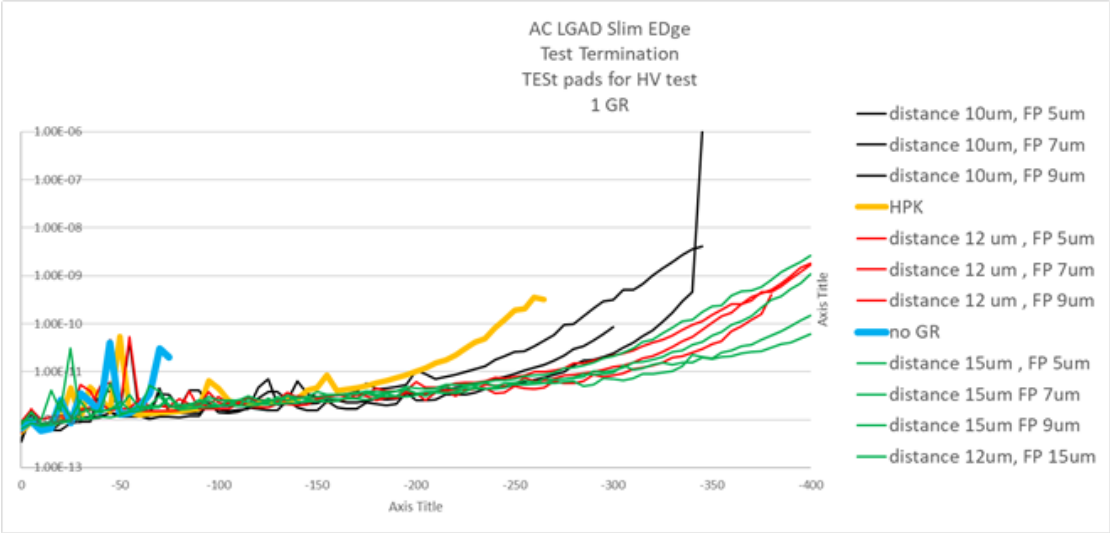


Figure 6: Current vs high voltage of pads as in Figure 5, fabricated on LGAD wafers, showing the voltage handling capability of these pads.

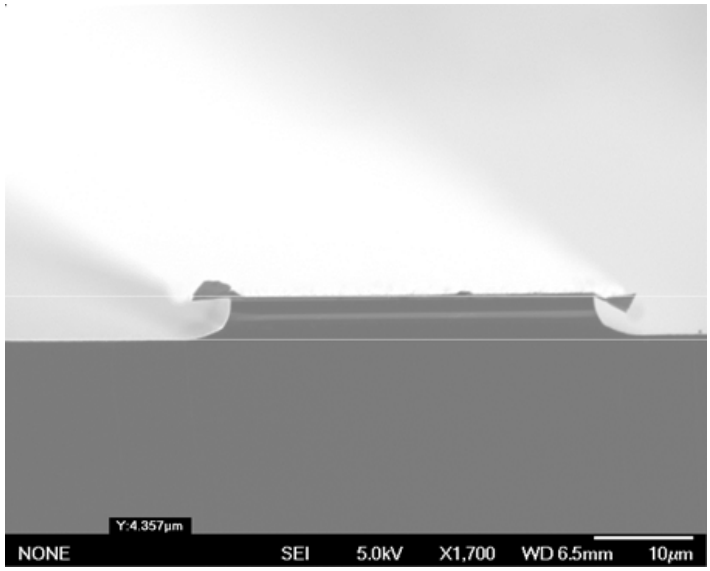


Figure 7: Trench test on a silicon wafer. Trench depth is 5 um, aluminum is used as an etch stop.

Based on those studies, we have started the design of the wafers for a new set of AC-LGADs for EIC, to study on a prototype the minimal possible edge size, different geometrical layouts, e.g. the number of pixel and pixel pitch, and optimise the charge sharing, see Figure 8.
The 4" wafer will be populated with devices having different dimensions, starting from many 1 x1 mm^2, useful to test several parameters (slim edge geometries, gain layer distances, etc), up

to 1.5 x 1.5cm^2. Intermediate dimension structures will be present as well, although safer design rules will be adopted for these, leaving more daring structures (as emerged from the testing of this production) for the next design.
As of now, just the first layers have been designed and the design will be finalized in the following months.

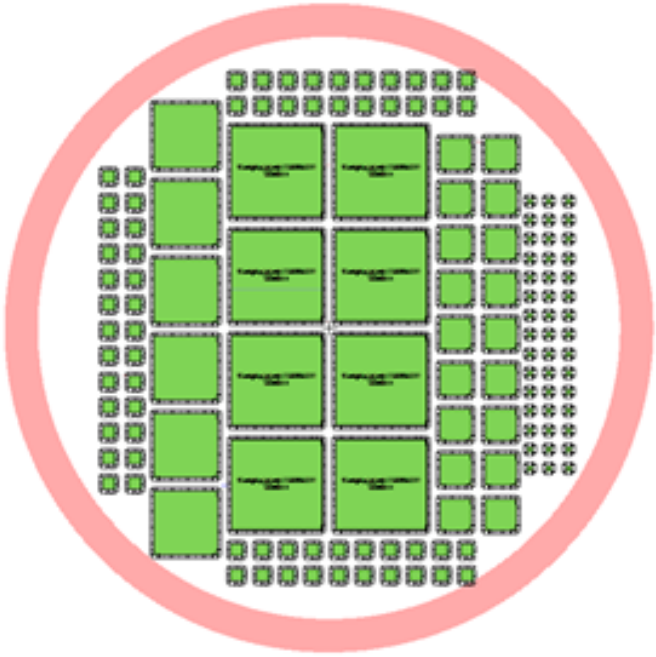


Figure 8: Layout of metal layer designed for the AC-LGAD wafers to be fabricated at BNL, which features several structures of different dimensions and pixel pitches.

In parallel we have started charge collection measurements of 3D sensors, kindly supplied by FBK (Italy), comparing them to PIN diodes (gain of 1) and LGADs. Being fabricated on 220 um thick silicon substrates, we expect these 3D sensors to have a collected charge of 2.8 fC, as compared to a charge 10-times higher in an LGAD with gain of about 50. Possibly because of the high capacitance of the 3D, our charge sensitive preamplifier was not able to measure the charge of the 3D sensor correctly, underestimating it. Another set-up is therefore is being prepared for future measurements.

A critical aspect for the development of a Roman Pot pixel detector with fast-timing capabilities is the readout. The front-end electronics must have timing and feature size compatible with those of the sensor. A fruitful discussion with ASIC designers that are developing fast-timing chips for the timing detectors at the HL-LHC has started. Current ASICs for ATLAS (ALTIROC) and CMS (ETROC) are designed in the CMOS TSMC 130 nm and CMOS 65 nm technologies respectively, and they use TDCs to measure the Time of Arrival and Time over Threshold, as well as RAM for data buffering. In the ALTIROC, for example, the maximum jitter is in the order of 25 ps for 10 fC charge, and the ALTIROC and ETROC total power consumption per unit area is about 200-300 mW / cm^2. As a comparison, the RD53 readout chip for pixel detectors for tracking (i.e. no timing) at the HL-LHC with 50 x 50 um^2 and 25 x 100 um^2 feature sizes is estimated to have a power density of about 1 W / cm2 or less. The ALTIROC and the ETROC chips host 225 and 256 channels respectively. Small pixels complicate the design due to limited space to accommodate TDCs and RAM and increased

preamp and TDC power density. However, from preliminary discussions it seems reasonable in a current HL-LHC ASIC design and with a limited effort from an expert ASIC designer to reach 500 x 500 um^2 feature size by rearranging blocks and removing components that are likely unnecessary in a Roman Pot detector (e.g. a large RAM), while maintaining the same timing performance.
In addition, by using Time-Over-Threhold (TOT) features in the ASICs, the charge sensed by pixel can be measured and in turn the charge sharing among pixels estimated. Therefore, using the TOT information the spatial resolution may improve beyond the fixed pixel pitch.
ASIC designers also reassure us that an edge size of about 50 um on three sides of the ASIC, i.e. where no wire bonding pads are present, is feasible. This edge size matches the value that we aim to achieve in the AC-LGAD sensors, and matches the physics performance specifications for Roman Pots close to the beam.

What was not achieved, why not, and what will be done to correct?

The studies that were planned for this period were successfully completed. However, detailed studies will continue in the next period to converge on the determination of the physics performance requirements, on the detector layout and on the charge sharing properties of AC-LGADs. For the latter the upcoming new wafer production will be important, as these properties will depend on the pixel size, pitch as well as other parameters, for example the doping of the resistive layer.
As reported earlier, charge collection measurements of the silicon 3D sensors have been so far unsuccessful, probably due to a suboptimal setup for readout. We plan to improve the setup and to measure 3D electrical and timing properties.

Future

What is planned for the next funding cycle and beyond? How, if at all, is this planning different from the original plan?

In the next period we plan to continue to further detail the physics studies to define the detector requirements and layout with further precision and confidence.
We will specifically focus on the requirements for the following very demanding physics processes

- The requirements for simultaneous detection of proton and neutron from deuterium in the RPs and the ZDC, respectively, to study short range correlations
- The detection of protons from nuclear breakup as veto for the breakup or to study saturation effects.

In parallel with physics performance studies, we will finalize the design for the next set of AC-LADs and we will start the wafer fabrication in the BNL silicon fabrication facility in Instrumentation Division.
In addition, we plan to study electrical and timing performance of alternative silicon sensor types, i.e. 3D sensors, used in pixel detectors at the LHC and HL-LHC, that have high radiation tolerance properties, and we will compare their performance to the one of AC-LGADs produced at BNL. The 3D sensors readout setup will be improved and we will use state-of-the art sensors provided by C. Da Via, co-investigator of this proposal and expert on 3D detectors.

What are critical issues?

A critical issue for the development of Roman Post at EIC is the readout of such fast-timing pixel detectors. As mentioned above, a discussion has started with ASIC designers for HL-LHC experiments to establish the most suitable solution in a short and medium term.

Additional information:

It will be useful in the future of project to include the expertise of a fast-time readout ASIC designer.

Manpower

Include a list of the existing manpower and what approximate fraction each has spent on the project. If students and/or postdocs were funded through the R&D, please state where they were located, what fraction of their time they spend on EIC R&D, and who supervised their work.

A.Tricoli: 10%; G. Giacomini: 10%; L. Lavitola (BNL summer student supervised by A. Tricoli and G. Giacomini): 50%; G. D'Amen (BNL Post. Doc., supervised by A. Tricoli at BNL): 20%.

0.15 FTE E.C. Aschenauer to supervise the simulations to determine the scientific requirements.
0.4 FTE of a PostDoc in the group of E.C. Aschenauer to perform the needed simulations.
0.25 FTE of a PhD student (W. Chang) in the group of E.C. Aschenauer to perform the needed simulations

External Funding

Describe what external funding was obtained, if any. The report must clarify what has been accomplished with the EIC R&D funds and what came as a contribution from potential collaborators.

No EIC funds have been spent at this point in time, as other available financial resources were leveraged for funding the personnel in physics simulation analysis, sensor testing as well as TCAD simulations and wafer design. These funds include A. Tricoli's Early Career Award and LDRD on fast-timing detectors
For the simulation part of the proposal we continue to utilize funds from the approved 3-year program development project "eRHIC: from Virtual to Real" of E.C. Aschenauer to support the labor needed to perform all the simulations.

Publications

Please provide a list of publications coming out of the R&D effort.

No publications yet.